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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JAGER, RYAN C	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/525,862	VAN DE BEEK ET AL.	
	Examiner	Art Unit	
	Ryan C. Jager	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8 and 9* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-9 are objected to because of the following informalities:

With respect to claim 1, it is suggested the recitation "said control signals" be changed to --said frequency control signals--.

Claims 2-6 are objected to because they contain the subject matter objected to in claim 1.

With respect to claim 2, it is suggested the recitation "a low-pass filter" on line 4, be changed to --the loop filter--, because the filter is already recited on line 10 of claim 1.

With respect to claim 6, it is suggested the recitation "a down frequency detector signals" be changed to --the down frequency detector signals--.

With respect to claim 7, it is suggested the recitation "the loop filter" be changed to --a loop filter--.

With respect to claim 7, it is suggested the recitation "phase detector" on line 12 be changed to --frequency detector--. The phase detector outputs frequency control signals while the frequency detector outputs frequency detector signals.

With respect to claim 7, it is suggested the recitation "and a down charge pump" on line 9 be changed to --and a down frequency detector signal coupled to a charge pump--.

With respect to claim 8, it is suggested the recitation "the third flip-flop" on line 11, be changed to --a third flip-flop--.

With respect to claim 9, it is suggested the recitation "the third flip-flop" on line 11, be changed to --a third flip-flop--.

With respect to claim 9, it is suggested the recitation "the output of the second flip-flop" on line 12, be changed to --a output of the second flip-flop--.

With respect to claim 9, it is suggested the recitation "the output of the first flip-flop" on line 12, be changed to --a output of the first flip-flop--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 8, the recitation "up and down frequency detector signals" on line 9, is indefinite because it is unclear if the up and down frequency detector signals are the same as the frequency detector signals on line 3 of claim 8 or in addition to them.

With respect to claim 9, the recitation "up and down frequency detector signals" on line 9, is indefinite because it is unclear if the up and down frequency detector signals are the same as the frequency detector signals on line 3 of claim 9 or in addition to them.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshita et al. (US Patent Application Publication 20020053950) in view of Atkinson (UK Patent Application, GB, 2253316).

With respect to claims 1 and 8, figure 1 of Takeshita et al. discloses a phase locked loop comprising a phase detector (11) for determining a phase difference between a reference signal (DATA) and relative phase shifted signals (QCLK, ICLK, I'CLK) to generate frequency control signals (UP, DOWN);

wherein the frequency control signals are coupled to a first charge pump (13); and a frequency detector (12, detail in figure 6) coupled to receive the reference signal and the relative phase shifted signals for supplying up and down frequency detector signals (127,128) to a second charge pump (14) communicatively coupled to a loop filter (C11), the frequency detector comprising a first flip-flop and a second flip-flop each communicatively coupled to the reference signal and to a different one of the relative phase shifted signals and a third flip-flop communicatively coupled to the output of the first and second flip-flops (figure 6, of Takeshita et al discloses a frequency detector with the a third flip-flop communitcatively coupled to the outputs of the first and second flip-flops).

Takeshita et al does not disclose the detail of the phase detector comprising means for obtaining a one of said frequency control signals by binary multiplication of the reference signal and one of the relative phase signals; means for obtaining a second one of said control signals by binary multiplication of the relative phase shifted signals,

However, figure 4 of Atkinson discloses a phase detector performing binary multiplication of mutually phase shifted signals and a reference signal to produce frequency

control signals to a charge pump. Therefore it would have been obvious to one skilled in the art at the time the invention was made to modify the PLL in figure 1 of Takeshita et al. by replacing the phase detector (11, figure 1) of Takeshita et al with the phase detector (A and B) in figure 4 of Atkinson for the purpose of eliminating the need for producing a third phase shifted signal in the splitter and reducing the number of electronic components used in the circuit.

With respect to claim 2,the above combination discloses a phase locked loop as claimed in claim 1, further comprising a splitter (17) for generating the relative phase shifted signals (ICLK, I'CLK, QCLK) the splitter having an input signal (174) generated by a voltage controlled oscillator (16) coupled to the first charge pump (13) and to a the low-pass filter (C11).

With respect to claim 6, the above combination discloses a phase locked loop as claimed in claim 1, wherein the up and the down frequency detector signals are generated using a binary multiplication of a signal from the output of the second flip-flop and a signal from the output of the first flip-flop (see figure 6, 38 and 39 both receive an output from the first and second flip-flops and generate the UP and DOWN signals).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshita et al. (US Patent Application Publication 20020053950) in view of Atkinson (UK Patent Application, GB, 2253316) and further in view of Nakamura (USP 6072370).

With respect to claim 3, the above combination teaches the use of a frequency divider followed by a phase splitter, providing feedback in a PLL to a phase detector performing binary multiplication of mutually phase shifted signals and a reference signal to produce frequency control signals to a charge pump. But the above modification does not disclose a divide by two

circuit with first and second bi-stable circuits. However, figure 7 of Nakamura discloses a divide-by-two circuit comprising a first and second bi-stable circuit for providing relative phase shifted feed back signals in a PLL. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace the phase splitter (176) in figure 1 of Takeshita et al. with the splitter in figure 7 of Nakamura for the purpose of reducing the size of the splitter circuit used in the PLL.

5. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshita et al. in view of Atkinson (UK Patent Application, GB, 2253316) and further in view of Dalmia (USP 6683930, filed 12/23/99)

With respect to claim 4, the above combination of Takeshita et al. and Atkinson discloses all the limitations of this claim except the splitter comprises a series coupling of a delay line and an inverter. However, figure 6 of Dalmia discloses a signal splitter comprising a delay line (300a-b) in series with an inverter (300c) (column 4 discloses a delay line of inverters capable of producing different desired phases of an input signal by adding more inverters). Therefore it would have been obvious to one skilled in the art at the time the invention was made to use a delay line of inverters to produce the desired phases of the input signal as output.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshita et al. in view of Atkinson and further in view of Dalmia (USP 6683930).

With respect to claim 5, the above combination of Takeshita et al. and Atkinson discloses all the limitations of this claim except for a quadrature oscillator providing the relative phase

shifted signals. However, figures 4 and 6 of Dalmia disclose the use of a quadrature oscillator capable of producing the relative phase shifted signals in quadrature for feedback in a PLL. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace the oscillator in the PLL of Atkinson with a quadrature oscillator for the purpose of eliminating the need for the splitter (13) and therefore making the circuit smaller.

Allowable Subject Matter

7. Claim 7 would be allowable if rewritten or amended to overcome the claim objections set forth in this Office action.

8. Claim 9 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Response to Arguments

9. Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Jager whose telephone number is (571) 272-7016. The examiner can normally be reached on M-F 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan C. Jager
10/26/2006

LONG NGUYEN
PRIMARY EXAMINER